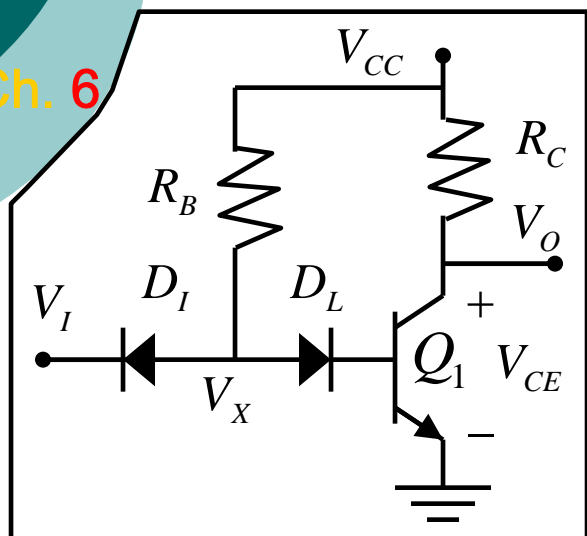Digital Electronics.

CHAPTER SIX

Diode-Transistor Logic [DTL]

Introduction

○ To improve upon the RTL circuits, DTL circuits are introduced in this chapter.

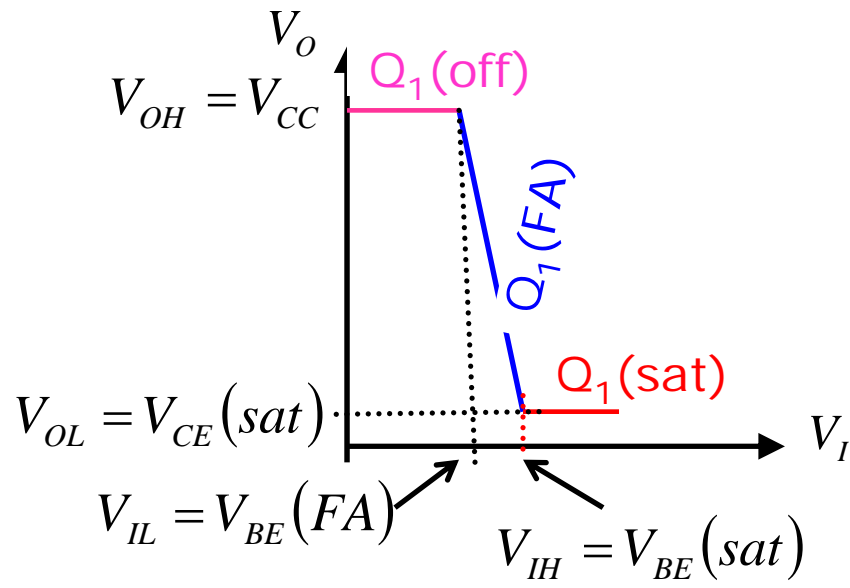○ The fan-out in RTL gates was relatively low.

Basic DTL Inverter

$$\text{For} \begin{cases} V_I - V_{DI}(ON) + V_{DL}(ON) < V_{BE}(FA) \\ V_I < V_{BE}(FA) \quad \Longrightarrow \quad \boxed{V_X < V_{BE}(FA) + V_{DI}(ON)} \\ \boxed{V_{IL} = V_{BE}(FA)} \qquad \boxed{V_{OH} = V_{CC}} \end{cases}$$

D_I is ON,
D_L & Q_1 are OFF

$$\text{For} \begin{cases} V_I = V_{BE}(FA) \quad \Longrightarrow \quad D_I \ \& \ D_L \ \& \ Q_1 \ \text{are ON (FA)} \\ \boxed{V_X = V_{BE}(FA) + V_{DL}(ON)} \end{cases}$$

$$\text{For} \begin{cases} V_I - V_{DI}(ON) + V_{DL}(ON) = V_{BE}(sat) \\ \boxed{V_{IH} = V_{BE}(sat)} \\ V_I \geq V_{IH} \quad \Longrightarrow \\ \boxed{V_{OL} = V_{CE}(sat)} \end{cases}$$

D_I is OFF,
D_L is ON
Q_1 is sat

V_O

Q_1(off)

$V_{OH} = V_{CC}$

Q_1(FA)

Q_1(sat)

$V_{OL} = V_{CE}(sat)$

V_I

$V_{IL} = V_{BE}(FA)$

$V_{IH} = V_{BE}(sat)$

Basic DTL NAND Gate
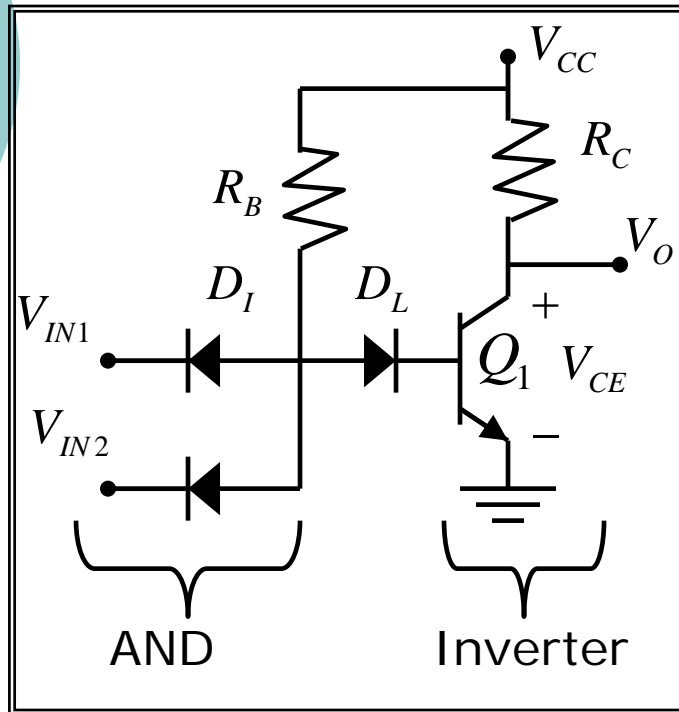
If at <u>least one input</u> less than $V_{BE}(FA)$, then Q_1 is off. i.e. $I_{CC}=0$
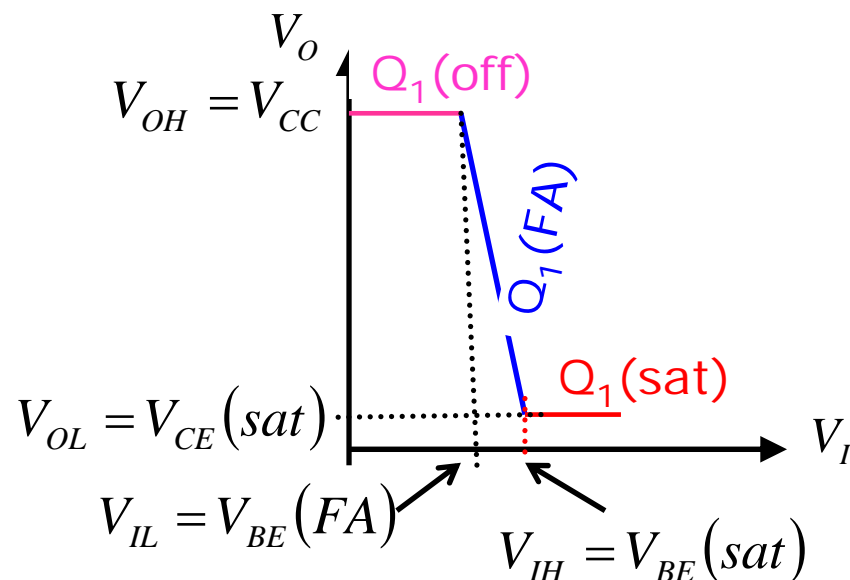
$$V_{OH} = V_{CC}$$

Noise Margins in DTL Gates

○ Noise margins:

- Low noise margin

$$V_{NML} = V_{IL} - V_{OL}$$

- High noise margin

$$V_{NMH} = V_{OH} - V_{IH}$$

$$V_{NML} = V_{BE}(FA) - V_{CE}(sat)$$

$$V_{NMH} = V_{CC} - V_{BE}(sat)$$

V_O

$V_{OH} = V_{CC}$ Q$_1$(off)

Q$_1$(FA)

Q$_1$(sat)
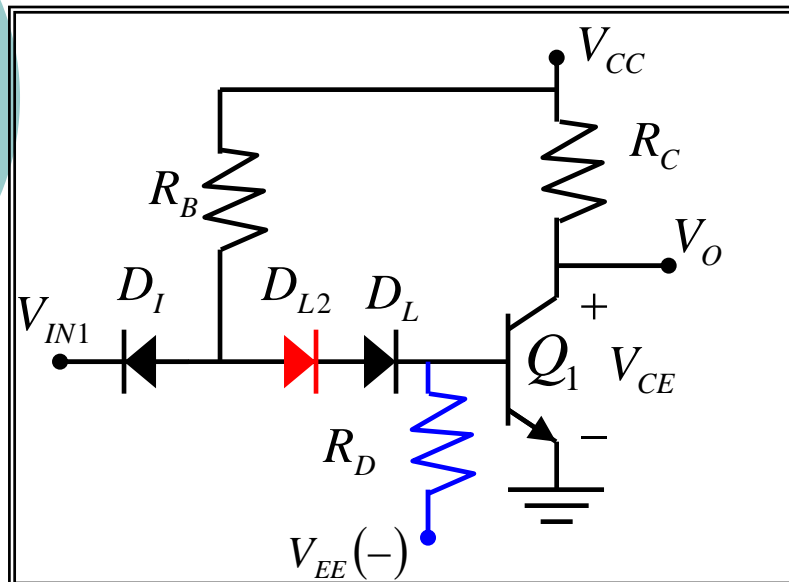
$V_{OL} = V_{CE}(sat)$

V_I

$V_{IL} = V_{BE}(FA)$

$V_{IH} = V_{BE}(sat)$

To <u>improve</u> the low noise margin, another diode is connected in series with D$_L$.

Level-Shifted DTL Inverter

The additional diode D_{L2} increases both V_{IL} and V_{IH} by $V_{DL2}(ON)$, i.e. The **VTC** shifts on the x-axis by $V_{DL2}(ON)$

Low noise margin is improved, while the high noise margin is still accepted.

Ex: $V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$, $V_{BE}(sat)=0.8V$, $V_{CC}=5V$,

When Q_1 is switched from saturation to cut-off, the stored base charges must be removed in order to make the switching faster. A resistor R_D & V_{EE} (-) are added.

Without D_{L2}	With D_{L2}
$V_{NML}=0.7-0.2$ $=0.5V$	$V_{NML}=1.4-0.2$ $=1.2V$
$\dfrac{1.2-0.5}{0.5}=140\%$	$140\%\ increase$
$V_{NMH}=5-0.8$ $=4.2V$	$V_{NMH}=5-1.5$ $=3.5V$
$\dfrac{3.5-4.2}{4.2}=16.7\%$	$16.7\%\ decrease$

Transistor Modified DTL

The fan-out can be furhter improved by replacing the level-shifting diode D_{L2} with a BJT Q_L, and splitting R_B into two resistors ρR_E and $(1-\rho)R_B$, whose sum is R_B.
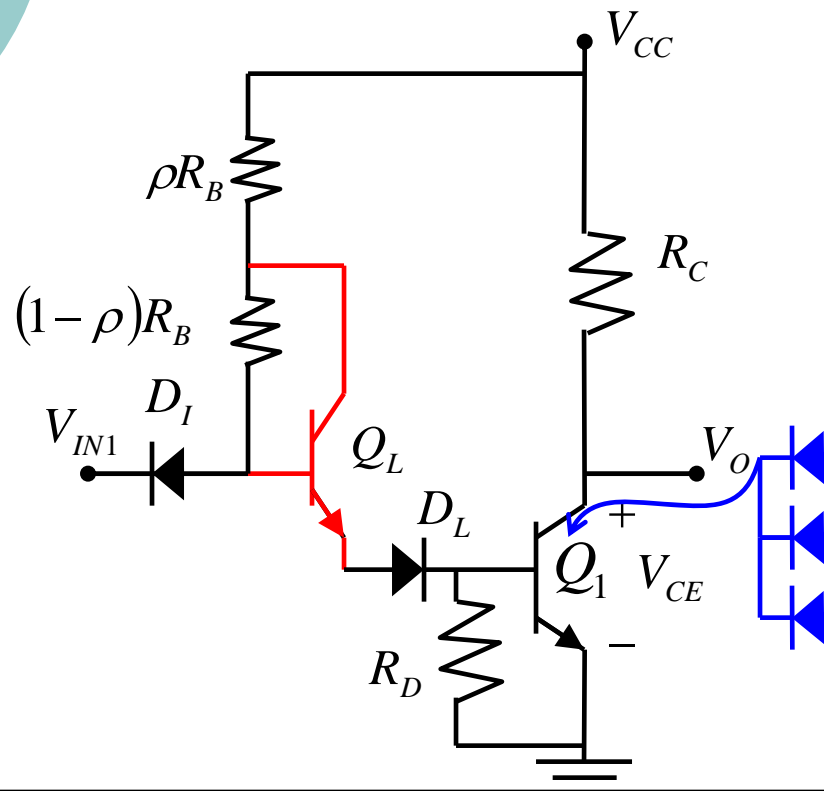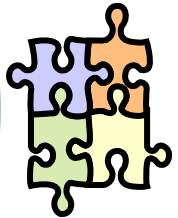

The BJT Q_L, provides more base current to Q_1., i.e. Q_1 sinks more current from an output load→ fan-out increases. Q_L operates in forward-active mode $(V_B < V_C)$ (emitter-follower configuration).

If $\rho = 1$, Q_L acts as a diode (D_{L2})

When splitting R_B: the input resistance R_B seen by V_{IN} (low) remains the same.

When $V < V_{IL}$: Q_L is ON (FA)

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Transistor Modified DTL

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○ Example

Determine V_{OH}, V_{OL}, V_{IL}, and V_{IH} for TMDTL , assuming $V_{CE}(sat)=0.2V$, $V_{BE}(FA)=0.7V$, $V_{CC}=5V$, $V_D(ON)=0.7V$
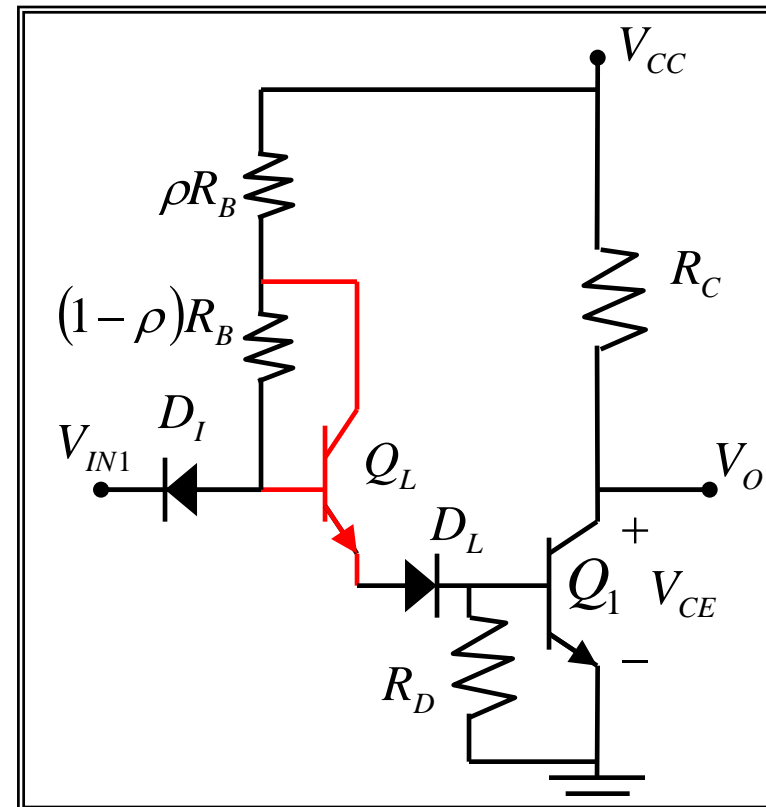
○ Solution

$$V_{OH} = V_{CC} \qquad V_{OL} = V_{CE}(sat)$$

$$V_{IL} = -V_{DI}(ON) + V_{BE,L}(FA) + V_{DL}(ON) + V_{BE,1}(FA)$$

$$V_{IL} = 1.4V$$

$$V_{IH} = -V_{DI}(ON) + V_{BE,L}(FA) + V_{DL}(ON) + V_{BE,1}(sat)$$

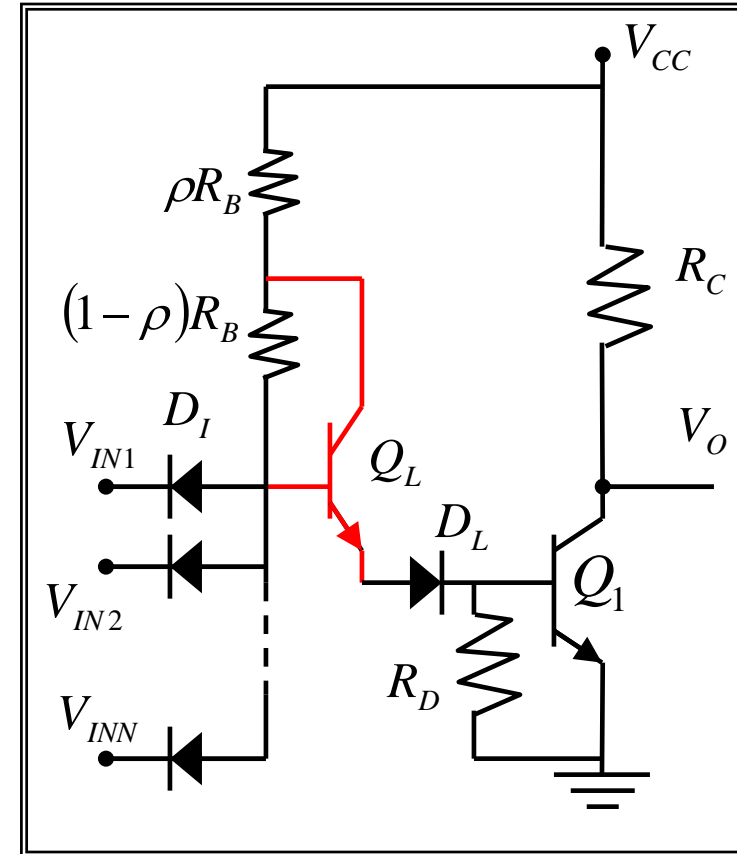$$V_{IH} = 1.5V$$

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DTL NAND Gate

The VTC is similar to the basic DTL NAND gate, (*refer to slide 5*)

When <u>any input</u> is low, then Q_L , Q_1 are off. Therefore, $V_{OH} = V_{CC}$.

When <u>all input</u> are high, then Q_L (FA), Q_1 (sat) are ON. Therefore,
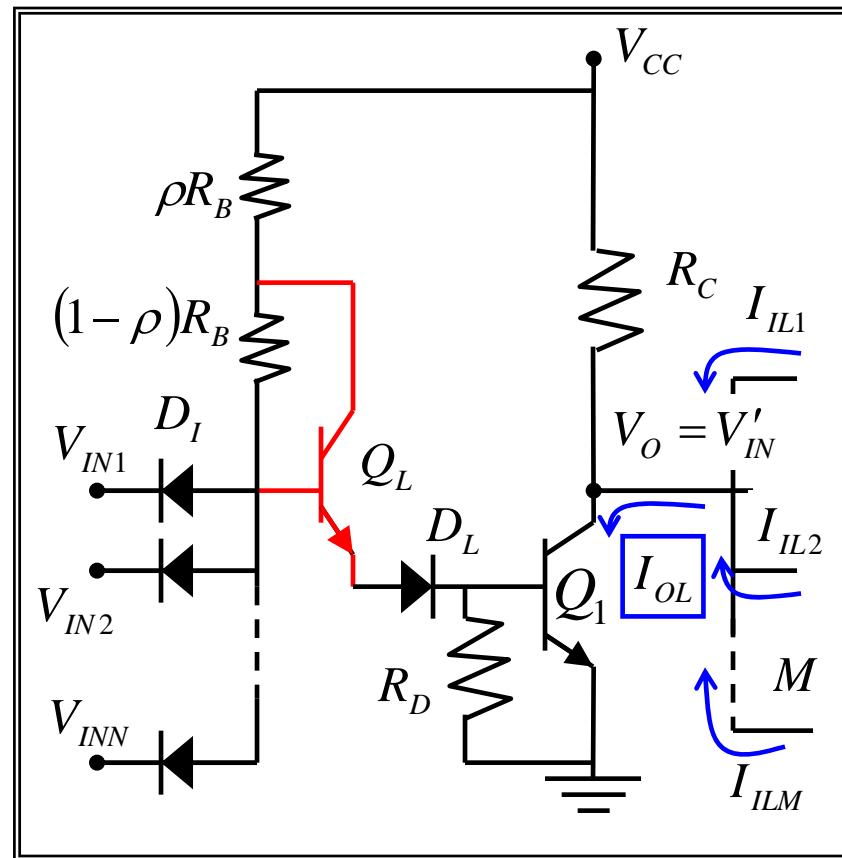$V_{OL} = V_{CE}$(sat).

When the output voltage is at state <u>high</u>, then the input diodes in the load gates are <u>reverse-biased</u>

When the output voltage is at state <u>low</u>, then the input diodes in the load gates are <u>forward-biased</u>

Maximum fan-out depends on the last statement
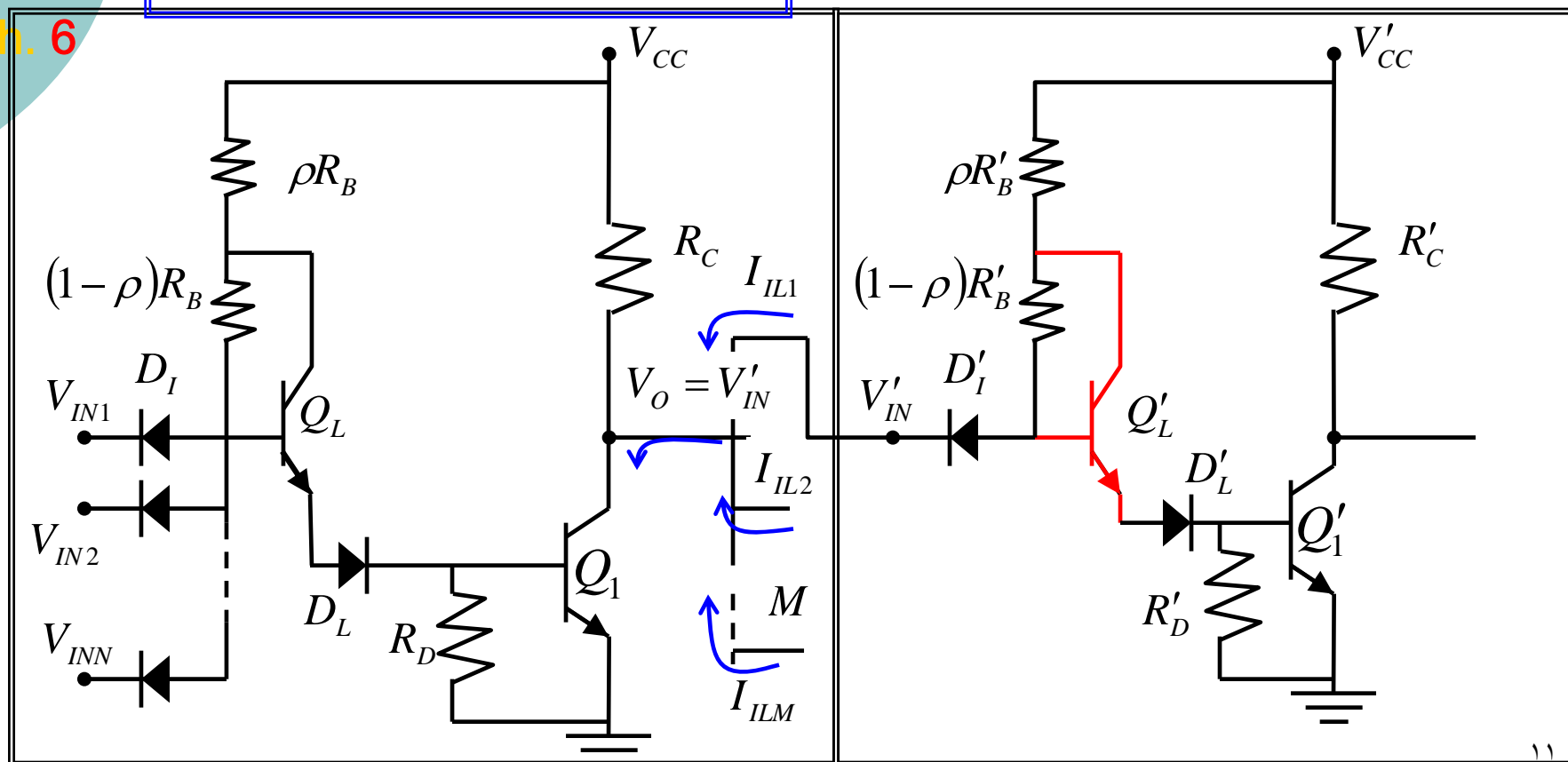
$$I_{OL} = M \times I_{IL}$$

$$M = \frac{I_{OL}}{I_{IL}}$$

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V_{CC}

ρR_B

$(1-\rho)R_B$

R_C I_{IL1}

D_I

V_{IN1} Q_L

$V_O = V'_{IN}$

D_L I_{IL2}

V_{IN2} Q_1 I_{OL}

R_D M

V_{INN}

I_{ILM}
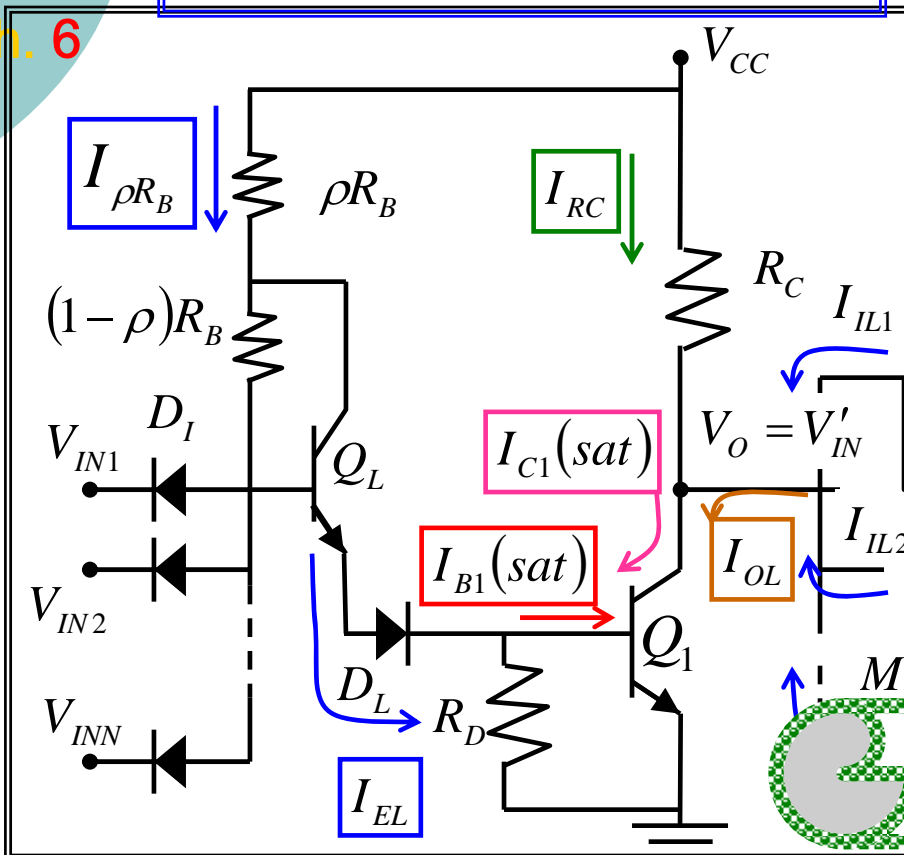
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DTL Fan-Out

Input current low I$_{IL}$

$$I_{IL} = \frac{V'_{CC} - V'_D(ON) - V_{CE}(sat)}{R'_B}$$

DTL Fan-Out

Input current low I_{IL}

$$I_{IL} = \frac{V'_{CC} - V'_D(ON) - V_{CE}(sat)}{R'_B}$$

Output current low I_{OL}

$$I_{OL} = I_{C1}(sat) - I_{RC}$$

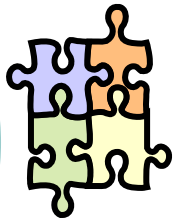$$I_{OL} = \sigma_1 \beta_F I_{B1}(sat) - \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

$$I_{B1}(sat) = I_{EL} - \frac{V_{BE}(sat)}{R_D}$$

$$I_{EL} = I_{\rho R_B}$$

Assuming IBL negligible, we can neglect the voltage drop across (1-ρ)R$_B$.

$$I_{\rho R_B} \cong \frac{V_{CC} - V_{BE,L}(FA) - V_D(ON) - V_{BE1}(sat)}{\rho R_B}$$

$I_{\rho R_B}$

ρR_B

I_{RC}

R_C

$(1-\rho)R_B$

D_I

V_{IN1}

Q_L

$I_{C1}(sat)$

$V_O = V'_{IN}$

$I_{B1}(sat)$

I_{OL}

I_{IL2}

V_{IN2}

D_L R_D

Q_1

M

V_{INN}

I_{EL}

V_{CC}

I_{IL1}

DTL Fan-Out

○ Example

Determine the maximum fan-out for driving DTL gate, assuming:
$V_{CE}(sat)=0.2V$, $V_{BE}(sat)=0.8V$,
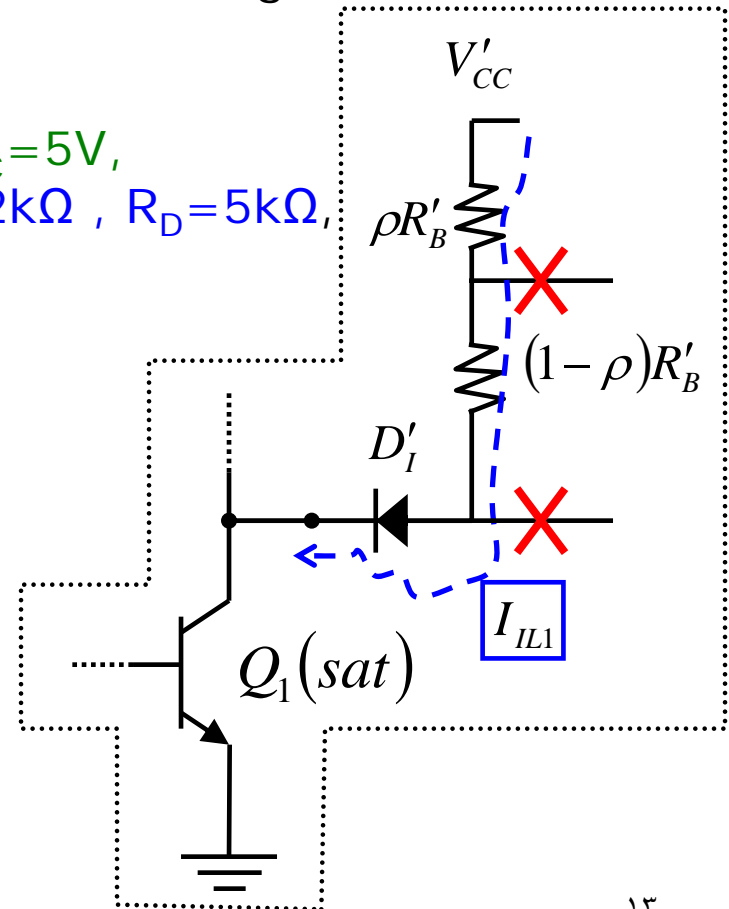$V_{BE}(FA)=0.7V$, $V_D(ON)=0.7V$, $V_{CC}=5V$,
$R_C=6k\Omega$, $\rho R_B=1.75k\Omega$, $(1-\rho)R_B=2k\Omega$, $R_D=5k\Omega$,
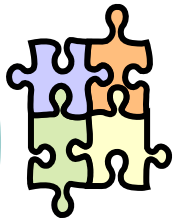$\beta_F=49$, and $\sigma_{1L}=0.85$.

○ Solution

$$I_{IL} = \frac{V'_{CC} - V'_D(ON) - V_{CE}(sat)}{R'_B}$$

$$I_{IL} = \frac{5-0.7-0.2}{3.75} = 1.093mA$$

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DTL Fan-Out

○ Example

Determine the maximum fan-out for driving DTL gate, assuming:
$V_{CE}(sat)=0.2V$, $V_{BE}(sat)=0.8V$,
$V_{BE}(FA)=0.7V$, $V_D(ON)=0.7V$, $V_{CC}=5V$,
$R_C=6k\Omega$, $\rho R_B=1.75k\Omega$, $(1-\rho)R_B=2k\Omega$, $R_D=5k\Omega$,
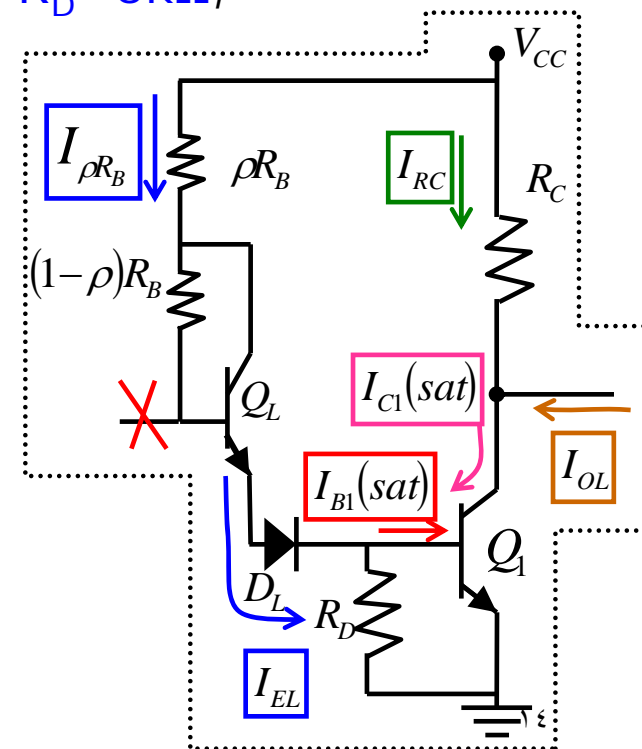$\beta_F=49$, and $\sigma_{1L}=0.85$.

○ Solution

$$I_{IL}=1.093mA$$

$$I_{\rho R_B} \cong \frac{V_{CC}-V_{BE,L}(FA)-V_D(ON)-V_{BE1}(sat)}{\rho R_B}$$

$$I_{\rho R_B} \cong \frac{5-0.7-0.7-0.8}{1.75}=1.6mA=I_{EL}$$

$$I_{B1}(sat)=I_{EL}-\frac{V_{BE}(sat)}{R_D}=1.6-\frac{0.8}{5}=1.44mA$$

$$I_{OL}=0.85\times49\times1.44-\frac{5-0.2}{6}=59.98-0.8=59.18mA$$

$$M=\frac{I_{OL}}{I_{IL}}=\frac{59.18}{1.093}=54.4 \qquad M=54$$

DTL Power-Dissipation

Output high current supplied ($I_{CC}(H)$)
For High output, Input is <u>low</u> ($V_{CE}(sat)$)

$$I_{\rho R_B}(H) \cong \frac{V_{CC} - V_D(ON) - V_{CE1}(sat)}{R_B}$$

Since Q_1 is cut-off, $I_{RC}(OH) = 0 \rightarrow I_{CC(Total)}(OH) = I_{\rho RB}(OH)$

Output low current supplied ($I_{CC}(L)$)
For Low output, Input is <u>High</u>

$$I_{\rho R_B}(L) \cong \frac{V_{CC} - V_{BE,L}(FA) - V_D(ON) - V_{BE1}(sat)}{\rho R_B}$$

$$I_{RC}(L) = \frac{V_{CC} - V_{CE}(sat)}{R_C}$$

$$I_{CC}(L) = I_{RC}(L) + I_{\rho RB}(L)$$

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- HW #6: Solve Problems: 6.1 , 6.5, 6.8, 6.12,6.14